ARGUMENTS/REMARKS

Applicants would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe and claim the subject matter which applicants regard as the invention.

The Examiner objected to various sections of the specification for errors. Applicant has amended those sections specifically objected to by the Examiner, making the objections moot.

Claims 1-30 remain in this application.

Claim 1 was again rejected under 35 U.S.C. §112, second paragraph for being incomplete. Again, applicant does not understand the Examiner's rejection. It again appears that the Examiner wants applicant to add additional steps to the claim. Applicant notes that all of the steps of the claim are part of a method for "analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation" as stated in the preamble, and thus no such step as recommended by the Examiner is necessary for completeness. Furthermore, the Examiner states, without providing any basis, that an "essential" step has been left out, and that the method terminates at the FFT processing step. Applicant disputes this characterization. The Examiner is referred to MPEP §2173.04 which makes clear that claims cannot be rejected merely because the Examiner does not agree with their breadth. Applicant is legally permitted to choose the breadth of the claims, and unless the Examiner finds that the claims read on prior art, the claims need not be narrowed for arbitrary reasons.

In addition, the term "comprising" is open ended, and thus does not imply that the method terminates at the FFT processing step (nor does it imply that it does not). Furthermore, the sequence of steps in an actual method is not implied merely by the order in which they are listed in the claims. Additional steps may well be part of an actual method as implemented, or may not, and other orders of the listed step are possible, and within the scope. It is enough that the applicant disclose only that which the applicant regards as the invention according to that particular claim. The fact that another claim specifies more steps does not matter. Applicant is allowed to specify claims in varying scope.

Thus, the Examiner should withdraw this rejection.

Claim 30 was also rejected under 35 U.S.C. §112 for being a method claim depending on a system claim. Claim 30 has been amended, making the rejection moot.

Claims 1 & 28 were rejected under 35 U.S.C. §102(a) (sic) as being anticipated by Hayashi *et al.* ("EMI Noise Analysis Under ASIC Design Environment") in view of Bonitz (U.S. 6,237,126). For the following reasons, the rejection is respectfully traversed.

First, applicant believes the rejection should have been under 35 U.S.C. §103, and will respond under that assumption.

Hayashi teaches only a simplification model for an electric source mesh (see page 18, col. 2, para. 4 to page 19, col. 1, para. 2). Hayashi does not disclose a concrete method to analyze EMI by a gate-level simulation. In contrast, the language of claims 1 and 28 recite calculating an instantaneous current amount using a gate-level current analysis method, and transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the calculated instantaneous current amount.

Hayashi presupposes a realization at the transistor level, and discloses only the *possibility* of applying a gate-level simulation to the EMI analysis, but does not teach any such procedure (and thus is not enabling). The reference teaches only a noise analysis system carried out at the *transistor* level, and does not teach operability at the gate level. Thus, Hayashi does not enable a gate-level analysis method.

In addition, Hayashi does not disclose the relationship between any gate-level simulation and EMI analysis. Specifically, Hayashi does not disclose any method to transform an instantaneous current amount into an instantaneous current.

Furthermore, Bonitz discloses only the instance name for all cells. It does not overcome the shortcomings of Hayashi. The invention discloses a method of transforming an instantaneous current "amount" into an instantaneous current "shape", for example. Accordingly, the invention introduces a way to utilize gate-level simulation for EMI analysis. The prior art gate-level simulation cannot be utilized for EMI analysis.

Accordingly, because the combination of references do not teach all of the limitations

of claims 1 and 28, they are patentable over the references.

Claims 2-27 and 29-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi in view of in view of Bonitz (U.S. 6,237,126), and further in view of one or more of Chen *et al.* ("Power supply Noise Analysis Methodology for Deep-submicron VLSI Chip Design"), Roethig (U.S. 5,835,380), Kuwano *et al.* (U.S. 6,253,354) Schaefer (U.S. 5,617,325), Kamiya *et al.* (U.S. 6,304,998), and Zarkesh et al. (U.S. 6,212,665). For the following reasons, the rejections are respectfully traversed.

First, none of the additional cited references overcome the shortcomings of Hayashi, identified above. Hence, claims 2-27 and 29-30 are patentable over the references for at least the same reasons as their parent claims.

In addition, Chen is directed toward predicting worst-case peak currents, and does not consider EMI noise. Thus, Chen treats current waveform to time-axis modeling in only a rough manner. Modeling the current peak is different from the actual current waveform.

Furthermore, although Chen and Roething may disclose triangular modeling, the references do not disclose any suggestion to apply triangular modeling to gate-level simulations in order to analyze EMI noise.

In addition, Kuwano does not disclose the method for calculating a drop of voltage for each event (i.e., transition time). Kuwano only discloses the voltage drop for a cell delay. There is, thus, no motivation for using a transition time in Kuwano.

Accordingly, the Examiner has not supported a prima facie case of obviousness. The Examiner has not provided the proper motivation for modifying Hayahsi. It is not proper to merely find a reference teaching a missing limitation and stating that adding that limitation would be "obvious" because it might provide some benefit. The Examiner must show that there is some suggestion or motivation to modify the reference (MPEP §2143.01). The prior art must suggest the desirability of the combination (Id.). The fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient, by itself, to establish prima facie obviousness (Id.), and merely listing an advantage of the combination is also not sufficient, as some rationale for combining the references must be found in the references themselves, or drawn from a convincing line of reasoning based on established scientific principles practiced by one skilled in the art that some advantage or beneficial result

would be produced by the combination (MPEP §2144). Such motivation cannot be found in the application itself, as such hindsight is impermissible; the facts must be gleaned from the prior art. (MPEP §2142, last paragraph).

As indicated by the Examiner's response to applicants prior arguments, it is clear that the Examiner is merely adding various features obtained from the secondary references to the teachings of the primary reference without providing the proper motivation for such a modification. For example, the Examiner states that Chen was cited only for using triangular waveforms to calculate the peak current, and not for teaching an EMI method. But what would motivate one reading Hayashi to add the peak current calculation means of Chen? Chen does not suggest use for an EMI method, and Hayashi does not suggest use of triangular waveforms to calculate peak current. Instead, the Examiner merely cites the benefits of Chen as motivation for adding Chen to the primary reference. If such were considered proper motivation, all references would be self-motivating (because all references provide some benefit). This is would prevent ANY new combination of known elements from being patentable, and that is clearly NOT the law. Thus, the Examiner has provided no motivation for combining the features.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 32796.

Respectfully submitted,

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December 30, 2004